REMARKS

Claims 1-16 are all the claims pending in the application.

I. Claim Rejections under 35 U.S.C. § 103(a)

A. Claims 1-3, 6-14 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagamasa et al. (U.S. 2004/0177215) in view Kawaura (US 6,886,069).

Claim 1, as amended, recites the features of a tamper resistant module that includes an internal memory having a usage area used by a program stored in the tamper resistant module; and a processing unit, wherein when requested by the program, the processing unit is operable to (i) assign an area in the nontamper resistant memory to the program, and (ii) generate, on the internal memory of the tamper resistant module, access information for the assigned area in the nontamper resistant memory. Applicants respectfully submit that the Nagamasa and Kawaura do not does not disclose or suggest at least the above-noted features recited in claim 1.

Regarding Nagamasa, Applicants note that this reference discloses the use of a multimedia card 110 which includes an IC card chip 150, a flash memory chip (i.e., non-volatile memory) 130, and a controller chip 120 (see Fig. 22 and paragraph [0042]). As shown in Fig. 26 of Nagamasa, the IC card chip 150 includes a CPU 158, a ROM 159, a RAM 160, and an EEPROM 162 (see paragraph [0043]).

As explained in Nagamasa, if data of a large size cannot be transmitted in a lump to the IC card chip 150 from a host apparatus 220, then the controller chip 120 selects the access to the flash memory chip 130 and temporarily stores the data into a security process buffer area 2114 having a large enough capacity (see paragraph [0052]). The controller chip 120 then divides the data into a size in which the data can be transmitted to the IC card chip 150, reads out the divided

data from the flash memory chip 130, and transmits the divided data to the IC card chip 150 step by step (see paragraph [0052]).

In the Office Action, the Examiner has taken the position that, in Nagamasa, that the EEPROM 162 of the IC card chip 150 corresponds to the "internal memory" recited in claim 1 (see Office Action at page 3).

As indicated above, however, Applicants note that claim 1 recites that the processing unit is operable to generate, on the internal memory of the tamper resistant module, access information for the assigned area in the nontamper resistant memory.

Regarding the above-noted claim language, as well as the Examiner's above-noted position that the EEPROM 162 corresponds to the "internal memory" of the tamper resistant module, Applicants respectfully submit that while the controller chip 120 of Nagamasa is able to access data that is temporarily stored in the flash memory chip 130, and transmit such data to the IC card chip 150 (see paragraph [0052]), that Nagamasa does not disclose or in any way suggest that access information for an assigned area in the flash memory chip 130 is generated on the EEPROM 162 of the IC card chip 150.

With respect to the Examiner's comments regarding the above-noted feature in the paragraph bridging pages 10-11 of the Office Action, Applicants point out to the Examiner that while Nagamasa may disclose the ability for the controller chip 120 to issue a read command to the flash memory chip 130, that such a read command does not in any way whatsoever result in access information for an assigned area in the flash memory chip 130 being generated on the EEPROM 162 of the IC card chip 150.

Based on the foregoing, Applicants respectfully submit that Nagamasa does not disclose,

suggest or otherwise render obvious at least the above-noted feature set forth in claim 1 which recites that the processing unit is operable to (i) assign an area in the nontamper resistant memory to the program, and (ii) generate, on the internal memory of the tamper resistant module, access information for the assigned area in the nontamper resistant memory.

Further, Applicants note that because Nagamasa does not disclose or suggest that access information is generated on the internal memory of the tamper resistant module, as described above, that Nagamasa clearly also does not disclose or suggest the feature recited in amended claim 1 which indicates that the assigned area in the nontamper resistant memory is for a portion of confidential data to be written in, the portion of confidential data being used by the program and read by referring to the access information existing in the internal memory of the tamper resistant module.

In view of the foregoing, Applicants respectfully submit that Nagamasa does not disclose, suggest or otherwise render obvious at least the above-noted features recited in claim 1. Further, Applicants respectfully submit that Kawaura does not cure the above-noted deficiencies of Nagamasa.

Accordingly, Applicants submit that claim 1 is patentable over the combination of Nagamasa and Kawaura, an indication of which is kindly requested. Claims 2, 3 and 6-14 depend from claim 1 and are therefore considered patentable at least by virtue of their dependency.

In addition, regarding claim 2, Applicants note that this claim recites that the internal memory stores a first area table indicating a location and a size of the usage area, and a second area table indicating a location and a size of the assigned area in the nontamper resistant

memory, and that the access information is the second area table.

With respect to the above-noted features recited in claim 2, Applicants note that the Examiner has taken the position in the Office Action that Fig. 21 of Nagamasa, as well as paragraphs [0051] and [0052] of Nagamasa, disclose such features (see Office Action at page 2). Applicants respectfully disagree.

In particular, Applicants point out to the Examiner that Fig. 21 of Nagamasa depicts the flash memory chip 130, not the IC card chip 150. In this regard, as discussed above in conjunction with claim 1, the Examiner has taken the position in the Office Action that the EEPROM 162 of the IC card chip 150 corresponds to the "internal memory" as recited in the claims.

Therefore, because claim 2 is drawn to the internal memory (which the Examiner indicated corresponds to the EEPROM 162) having stored thereon a first area table and a second area table, Applicants note that the Examiner's position in the Office Action that the flash memory chip 130 includes the claimed "first area table" and "second area table" is inconsistent with the language set forth in claim 2.

Accordingly, Applicants submit that Nagamasa does not disclose, suggest or otherwise render obvious the above-noted features recited in claim 2. In addition, Applicants submit that Kawaura fails to cure this deficiency of Nagamasa. As such, Applicants submit that claim 2 is patentable over the cited prior art, an indication of which is kindly requested.

If the Examiner maintains the rejection of claim 2, Applicants kindly request that the Examiner explicitly identify the elements in Nagamasa that are being relied upon as corresponding to the claimed "first area table" and "second area table".

Regarding claim 16, Applicants note that this claim has been amended so as to recite that the controlling program is operable to (i) assign an area in the nontamper resistant memory to the application, and (ii) generate, on the internal memory of the tamper resistant module, access information for the assigned area in the nontamper resistant memory, wherein the assigned area in the nontamper resistant memory is for a portion of confidential data to be written in, the portion of confidential data being used by the program and read by referring to the access information existing in the internal memory of the tamper resistant module.

For at least similar reasons as discussed above with respect to claim 1, Applicants respectfully submit that the combination of Nagamasa and Kawaura does not disclose, suggest or otherwise render obvious the above-noted combination of features recited in claim 16. Accordingly, Applicants submit that claim 16 is patentable over the cited prior art, an indication of which is kindly requested.

B. Claims 4 and 5 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagamasa et al. in view of Kawaura, and further in view of Madoukh (U.S. 2001/0019614).

Claims 4 and 5 depend from claim 1. Applicants submit that Madoukh fails to cure the deficiencies of Nagamasa et al. and Kawaura, as discussed above, with respect to claim 1. Accordingly, Applicants submit that claims 4 and 5 are patentable at least by virtue of their dependency.

C. Claim 15 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagamasa et al. in view of Kawaura, and further in view of Deo et al. (U.S. 5,721,781).

Claim 15 depends from claim 1. Applicants submit that Deo fails to cure the deficiencies of Nagamasa et al. and Kawaura, as discussed above, with respect to claim 1. Accordingly, Applicants submit that claim 15 is patentable at least by virtue of its dependency.

II. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Hiromi EBARA et al.

/Kenneth W. Fields/
2008.07.23 17:16:19 -04'00'

By: _____
Kenneth W. Fields
Registration No. 52,430
Attorney for Applicants

KWF/krg
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
July 23, 2008